LISTING OF THE CLAIMS:

This Listing of the Claims replaces all previous versions of the claims. Please amend the claims as follows.

1. (currently amended) A method ~~for computing state data of~~ in an emulation system, comprising ~~steps of~~:

receiving a first sample of state data;

~~sorting~~ selecting data of interest from the first sample, wherein the data of interest is a subset of bits of the first sample and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest;

determining if residual storage space in a first buffer exists; and

storing ~~at least a portion of~~ the data ~~sorted~~ of interest from the first sample in said first buffer if it is determined that residual storage space in the first buffer exists, such that the first and second portions of the data of interest as stored is no longer separated from each other by the at least one bit, and otherwise storing said ~~portion~~ data of interest in ~~at least one other~~ a second buffer such that the first and second portions of the data of interest as stored are no longer separated from each other by the at least one bit.

2. (original) The method of claim 1, further comprising a step of determining whether the first buffer is full after storing the sorted first sample in the first buffer.

Claims 3-7. (canceled).

8. (original) The method of claim 1, further comprising steps of:

receiving a second sample of state data;

sorting the second sample; and

storing the sorted second sample.

9. (original) The method of claim 8, wherein the step of storing the sorted second sample comprises:

determining if residual storage space in the first buffer exists after storing the sorted first sample; and

storing at least a portion of the sorted second sample in the first buffer if residual storage space in the first buffer exists after storing the sorted first sample.

10. (currently amended) The method of claim 1, wherein receiving comprises receiving the first sample of state data ~~is received~~ from a reconfigurable emulation resource.

Claims 11-15. (canceled).

16. (original) The method of claim 1, further comprising a step of storing information associated with the first sample.

17. (currently amended) The method of claim 16, wherein the information comprises a bit position of the data of interest of the first sample.

18. (original) The method of claim 16, wherein the information comprises an identification of a pin associated with the first sample.

19. (original) The method of claim 16, further comprising steps of:
receiving a second sample of state data;
storing the second sample;
storing information associated with the first sample in memory; and
storing information associated with the second sample in memory.

20. (currently amended) An apparatus, comprising:

a first select logic device configured to receive samples of state data, to ~~sort samples of state data, and to~~ select data of interest from each of the samples of state data, the data of interest

having non-contiguous bits, and to sort the data of interest such that the non-contiguous bits become contiguous;

first and second buffers coupled to the first select logic device and configured to receive the ~~selected~~ sorted data of interest in an alternating manner by filling ~~one buffer and then the other~~the first and second buffers in an alternating manner;

a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer; and

an output storage device coupled to the second select logic device and configured to receive data drained from the selected ~~buffer~~one of the first and second buffers.

21. (original) The apparatus of claim 20, wherein the first select logic comprises a multiplexer.

22. (original) The apparatus of claim 20, wherein the second select logic device comprises a multiplexer.

23. (currently amended) The apparatus of claim 20, wherein the first select logic device ~~sends~~ is configured to send the data of interest to the second buffer ~~when~~ responsive to the first buffer ~~becomes~~ becoming full.

24. (original) The apparatus of claim 20, wherein the first select logic device comprises a data of interest sorter.

25. (previously presented) The apparatus of claim 20, further comprising:

a memory configured to store information associated with the samples of state data.

26. (previously presented) The apparatus of claim 25, wherein the information comprises at least a bit position of data of interest of the sample of state data.

27. (previously presented) The apparatus of claim 25, wherein the information comprises an identification of a pin associated with each of the samples of state data.

28. (previously presented) The apparatus of claim 20, wherein the output storage device is configured to store information associated with each of the samples of state data.

29. (original) A method for associating trace data chains with pins of an integrated circuit, the method comprising steps of:

determining a trace data fill rate of each of a plurality of trace data chains; and

determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates.

30. (original) In an emulation debugging resource, a method comprising steps of:

determining fill rates of a plurality of trace data chains;

determining a schedule for associating a plurality of pins with the plurality of trace data chains based at least upon the determined fill rates; and

associating a set of the plurality of trace data chains with the plurality of pins in accordance with the determined schedule.

31. (previously presented) In an integrated circuit, the integrated circuit including an emulator, an apparatus comprising:

a plurality of trace data chains;

a trace pin select logic device coupled to the plurality of trace data chains to select a set of the plurality of trace data chains;

a plurality of pins; and

a memory coupled to the trace pin select logic device and configured to store a schedule to associate the selected set with the pins based at least upon determined trace data chain fill rates of the set.

32. (new) The method of claim 1, further comprising:

receiving a second sample of state data;

selecting data of interest from the second sample, wherein the data of interest of the second sample is a subset of bits of the second sample and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest of the second sample; and

storing the data of interest from the second sample in one of said first and said second buffer such that the first and second portions of the data of interest as stored are no longer separated from each other by the at least one bit and such that the data of interest from the second sample is stored so as to be contiguous with the stored data of interest from the first sample.